In the Specification:

Please amend the paragraph beginning on page 5, line 30 as follows:

FIG. 3 illustrates an output-compensated buffer **140** according to an embodiment of the present invention. The output-compensated buffer **140** includes a buffer circuit **7** and a feedback circuit **8**. The buffer circuit [[**8**]] 7 includes an input terminal **2**, an output terminal **4**, a control terminal **6**, and a bias terminal ~~**10**~~ **N3**. As illustrated, the buffer circuit [[**8**]] 7 includes a single source follower circuit including first and second NMOS transistors **M11** and **M12**. The first NMOS transistor **M11** has a gate terminal that receives an input signal **Vin** at the input terminal **2** and a source terminal connected to the drain terminal of the second NMOS transistor **M12** . The first NMOS transistor **M11** also has a drain terminal connected to a resistor **R1** at a node **N3**, with the resistor **R1** also being connected to a power source **VDD**, such that a secondary power supply voltage **VDD'** is applied to the drain terminal of the first NMOS transistor **M11**. The second NMOS transistor has a gate terminal that receives a control signal **Vg** applied at the control terminal **6** and a source terminal connected to a signal ground **GND**. In the source follower configuration shown, the first NMOS transistor **M11** serves as a driving transistor, while the second NMOS transistor ~~**M21**~~ **M12** serves as a load transistor.

Please amend the paragraph beginning on page 6, line 27 as follows:

FIG. 4 illustrates an output compensated buffer **140'** according to another embodiment of the present invention. The output-compensated buffer **140'** includes a buffer circuit **7'** with an input terminal **2'**, an output terminal **4'**, a control terminal **6'** and a bias terminal ~~**10'**~~ **N4**. The buffer circuit **7'** has a 3-stage structure including an input source follower circuit **14** and additional second and third stage source follower circuits **10**, **12**. The input source follower circuit **14** includes driving and load NMOS transistors **M21**, **M22**. A gate terminal of the driving transistor **M21** receives an input signal **Vin** applied at the input terminal **2'**, and has a source terminal connected to the

drain terminal of the load transistor **M22**. The gate terminal of the load transistor **M22** receives a control signal **Vg** applied at the control input **6'**. The drain terminal of the driving transistor is connected to one terminal of a resistor **R2** at a node **N4**. The resistor **R2** has a second terminal connected at to a power source **VDD**, such that a secondary power supply voltage **VDD'** is applied to the drain terminal of the driving transistor **M21**.